REMARKS

This responds to the Office Action mailed on March 20, 2006, and the references cited therewith.

Claims 7, 12-15 and 22 are amended, claims 9-11 and 23 are canceled, and claims 29-32 are added; as a result, claims 7-8, 12-15, 22, 24-25 and 29-32 are now pending in this application.

Affirmation of Election

Restriction to one of the following claims was required:

I. Claims 1-6 and 26, drawn to method and processing unit for executing memory instructions by creating a physical address and using the address to access either a local or remote cache, classified in class 711, subclasses 122 and/or 214.

II. Claims 7-15 and 22-25, drawn to a method and a processor for storing memory requests into different queues based on whether or not the memory requests hit in the local cache, classified in class 711, subclass 118.

III. Claims 16-21 and 27-28, drawn to a method and processing unit for synchronizing and caching scalar and vector memory instructions, classified in class 712, subclass 218.

As provisionally elected by Applicant's representative, Thomas F. Brennan, on February 24, 2006, Applicant elects to prosecute the invention of Group II, claims 7-15 and 22-25

The claims of the non-elected inventions, claims 1-6, 16-21, and 26-28, are hereby withdrawn. However, Applicant reserves the right to later file continuations or divisions having claims directed to the non-elected inventions.

§102 Rejection of the Claims

Claims 7-13, 22 and 23 were rejected under 35 U.S.C. § 102 (b) for anticipation by Hughes (US 6,393,536).

Hughes describes a load/store of a scalar processor employing a last-in-buffer indication which identifies whether or not the store in that entry is the youngest store in the buffer to update the memory locations specified by the corresponding store address. Specifically Hughes describes a load/store unit including two buffers, LS1 and LS2, for storing memory operations and two control logics attached to the buffers.

Although Hughes describes a controlling mechanism using 'hit/miss' conditions in a data cache (28) for determining in which of the two buffers the memory operation should be fulfilled, Hughes does not teach or suggest processing a memory request by comparing an address to addresses within local cache while, at the same time, comparing the address to partial addresses stored in an FOQ as taught by Applicant and claimed in claim 7 and 22. This is important to maintain proper request ordering in a scalar processor as described in the lines 10-15 of the Specification.

Firstly, under Hughes approach, for example, the memory operations are moved from LS1 buffer (60) to LS2 buffer (62) subsequent to probing data cache (28) independent of the probe status (e.g. hit/miss, etc.) (col. 14, lines 24~27). Hughes further states that "all memory operations are placed into LS2 buffer 62 after an initial probe of data cache 28" (col. 16, lines 62~63).

This contrasts with Applicant's approach, where some of the memory requests are not sent to the second memory request container after checking a cache. For example, as disclosed in lines 3~19 of the Specification, read requests [from the IRQ] that hit in the Dcache and have no potential matches in the FOQ are serviced immediately and are not sent to the FOQ.

Accordingly, under Hughes approach, LS2 buffer is not checked along with the data cache (28) at the same time when the memory request is issued from LS1 buffer (60) to determine whether or not the memory request is sent to LS2 buffer (62).

This teaches away Applicant's teaching that not only a cache but also the second FOQ is checked at the same time upon a memory request from the IRQ to determine whether or not the memory request is entered into the FOQ as described and claimed by Applicant (Spec. p. 16, line 24 ~ p. 17, line 19).

Furthermore, Hughes does not teach or suggest specific embodiment of a load/store unit which, for example, includes routing a subsequent memory request from the IRQ to the FOQ if the memory request matches the partial address of any valid entry in the FOQ as described (Spec. p. 17, lines 9~20) and claimed in claim 7 by Applicant.

In conclusion, unlike the Examiner's assertion, Hughes does not teach or suggest processing a memory request as in both the IRQ and FOQ depending on two conditions, hit/miss in the cache and a potential match in the FOQ, as taught by Applicant and claimed in claim 7 and 22. Claims 7 and 22 have been amended to emphasize these differences. Reconsideration is respectfully requested.

With regard to claims 8, 9, 11 and 23, these claims are patentable as being dependent on a patentable base claim.

§103 Rejection of the Claims

Claims 14 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hughes in view of Yamahata (US 5,247,639).

Claims 24 and 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hughes.

With regard to claims 14 and 15, these claims are patentable as being dependent on a patentable base claim. In addition, neither Hughes nor Yamahata, alone or in combination, teach or suggest processing the memory request in the FOQ when local cache processing is bypassed as taught by Applicant and claimed in claims 14 and 15.

With regard to claims 24 and 25, these claims are patentable as being dependent on a patentable base claim.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date August 21, 2006

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 21 day of August 2006.

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